IN THE CLAIMS

Claims 18 and 24 have been amended to reflect the change recommended by the Examiner.

Claim 1. (ORIGINAL) A circuit for timing the start of a precharge period in an eDRAM comprising:

a delayed lock loop circuit for receiving a clock signal and generating a control signal for adjusting an internal delay of said clock signal; and

means for generating a delayed clock signal in response to said control signal.

Claim 2. (ORIGINAL) The circuit of claim 1, wherein said means for generating said delayed clock signal is a multiple stage delay circuit, each stage of said multiple delay stage circuit connected in series and each stage individually responsive to said control signal.

Claim 3. (ORIGINAL) The circuit of claim 2, wherein each stage includes a inverter having an input and an output and a multiplicity of capacitors connectable between said output of said inverter and ground by pass gates; each pass gate responsive to a different bit of said control signal.

Claim 4. (ORIGINAL) The circuit of claim 2, further including means for further delaying said delayed clock signal in response to a fuse signal generated by a fuse bank circuit based on a pattern of blown and un-blown fuses in a fuse bank.

Claim 5. (ORIGINAL) The circuit of claim 1, wherein said means for generating said delayed clock signal is a set of multiple stage delay circuits and includes means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each

stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage circuit individually responsive to said control signal, said means for selecting responsive to a fuse signal generated by a fuse bank circuit based on a pattern of blown and un-blown fuses in a fuse bank.

Claim 6. (ORIGINAL) The circuit of claim 5, wherein each delay stage includes a inverter having an input and an output and a multiplicity of capacitors connectable between said output of said inverter and ground by pass gates, each pass gate responsive to a different bit of said control signal.

Claim 7. (ORIGINAL) The circuit of claim 5, further including means for further delaying said delayed clock signal in response to an additional fuse signal generated by an additional fuse bank circuit based on a pattern of blown and un-blown fuses in an additional fuse bank.

Claim 8. (ORIGINAL) The circuit of claim 1, wherein said delayed clock signal enables the start of said precharge period of said eDRAM.

Claim 9. (ORIGINAL) A method for timing the start of a precharge period in an eDRAM comprising:

providing a delayed lock loop circuit for receiving a clock signal and generating a control signal for adjusting an internal delay of said clock signal; and

providing means for generating a delayed clock signal in response to said control signal.

Claim 10. (ORIGINAL) The method of claim 9, wherein said means for generating said delayed clock signal is a multiple stage delay circuit, each stage of said multiple delay stage circuit connected in series and each stage individually responsive to said control signal.

Claim 11. (ORIGINAL) The method of claim 10, wherein each stage includes a inverter having an input and an output and a multiplicity of capacitors connectable between said output of said inverter and ground by pass gates; each pass gate responsive to a different bit of said control signal.

Claim 12. (ORIGINAL) The method of claim 10, further including further delaying said delayed clock signal in response to a fuse signal generated by a fuse bank circuit based on a pattern of blown and un-blown fuses in a fuse bank.

Claim13. (ORIGINAL) The method of claim 9, wherein said means for generating said delayed clock signal is a set of multiple stage delay circuits and includes means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage circuit individually responsive to said control signal, said means for selecting responsive to a fuse signal generated by a fuse bank circuit based on a pattern of blown and un-blown fuses in a fuse bank.

Claim 14. (ORIGINAL) The method of claim 13, wherein each stage includes a inverter having an input and an output and a multiplicity of capacitors connectable between said output of said inverter and ground by pass gates; each pass gate responsive to a different bit of said control signal.

Claim 15. (ORIGINAL) The method of claim 13, further including delaying said delayed clock signal in response to an additional fuse signal generated by an additional fuse bank circuit based on a pattern of blown and un-blown fuses in an additional fuse bank.

Claim 16. (ORIGINAL) The method of claim 15, wherein said pattern of blown and un-blown fuses and said additional pattern of blown and un-blown fuses is determined by scanning in test

patterns into a scan chain coupled to said fuse bank and said additional fuse bank and measuring the performance of said eDRAM.

Claim 17. (ORIGINAL) The method of claim 1, wherein said delayed clock signal enables the start of said precharge period in said eDRAM.

Claim 18. (CURRENTLY AMENDED) An eDRAM comprising:

an array of memory cells interconnected by wordlines and bitlines;

a delayed lock loop circuit for receiving a clock signal and generating a control signal for adjusting an internal delay of said clock signal;

means for generating first, second, third and fourth delayed clock signals in response to said control signal;

a wordline driver for activating wordlines in said eDRAM in response to an address signal, said wordline driver responsive to said third delayed clock signal;

a sense amplifier circuit for amplifying data signals on said bitlines, said sense amplifier circuit responsive to said first delayed clock signal and said second delayed clock signal;

a bitline precharge circuit for precharging said bitlines, said bitline ~~recharge~~ precharge circuit responsive to said third delayed clock ; and

a column select circuit for selecting particular bitlines to connect to means for outputting data signals from said array, said column select circuit responsive to said second delayed clock signal and said means for outputting data signals responsive to said fourth delayed clock signal.

Claim 19. (ORIGINAL) The circuit of claim 18, wherein said means for generating said first, second, third and fourth delayed clock signals are multiple stage delay circuits, each stage of each multiple delay stage circuit connected in series and each stage individually responsive to said control signal.

Claim 20. (ORIGINAL) The circuit of claim 19, wherein each stage includes a inverter having an input and an output and a multiplicity of capacitors connectable between said output of said inverter and ground by pass gates, each pass gate responsive to a different bit of said control signal.

Claim 21. (ORIGINAL) The circuit of claim 18, wherein said fourth delayed clock signal is delayed more than said third delayed clock signal, said third delayed clock signal is delayed more than said second delayed clock signal and second delayed clock signal is delayed more than said first delayed clock signal.

Claim 22. (ORIGINAL) The circuit of claim 18, wherein said means for generating said first, second, third and fourth delayed clock signals comprises:

a first set of multiple stage delay circuits and first means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage circuit individually responsive to said control signal, said means for selecting responsive to a first fuse signal generated by a first fuse bank circuit based on a pattern of blown and un-blown fuses in a first fuse bank;

a second set of multiple stage delay circuits and second means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage

circuit individually responsive to said control signal, said means for selecting responsive to a second fuse signal generated by a second fuse bank circuit based on a pattern of blown and un-blown fuses in a second fuse bank;

a third set of multiple stage delay circuits and third means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage circuit individually responsive to said control signal, said means for selecting responsive to a third fuse signal generated by a third fuse bank circuit based on a pattern of blown and un-blown fuses in a third fuse bank; and

a fourth set of multiple stage delay circuits and fourth means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage circuit individually responsive to said control signal, said means for selecting responsive to a fourth fuse signal generated by a fourth fuse bank circuit based on a pattern of blown and un-blown fuses in a fourth fuse bank.

Claim 23. (ORIGINAL) The circuit of claim 18, further including:

first means for further delaying said first delayed clock signal in response to a first additional fuse signal generated by a first additional fuse bank circuit based on a pattern of blown and un-blown fuses in a first additional fuse bank;

second means for further delaying said second delayed clock signal in response to a second additional fuse signal generated by a second additional fuse bank circuit based on a pattern of blown and un-blown fuses in a second additional fuse bank;

third means for further delaying said third delayed clock signal in response to a third additional fuse signal generated by a third additional fuse bank circuit based on a pattern of blown and un-blown fuses in a third additional fuse bank; and

fourth means for further delaying said fourth delayed clock signal in response to a fourth additional fuse signal generated by a fourth additional fuse bank circuit based on a pattern of blown and un-blown fuses in a fourth additional fuse bank.

Claim 24. (CURRENTLY AMENDED) A method of synchronous control of an eDRAM comprising an array of memory cells interconnected by wordlines and bitlines, said method comprising:

providing a delayed lock loop circuit for receiving a clock signal and generating a control signal for adjusting an internal delay of said clock signal;

providing means for generating first, second, third and fourth delayed clock signals in response to said control signal;

providing a wordline driver for activating wordlines in said eDRAM in response to an address signal, said wordline driver responsive to said third delayed clock signal;

providing a sense amplifier circuit for amplifying data signals on said bitlines, said sense amplifier circuit responsive to said first delayed clock signal and said second delayed clock signal;

providing a bitline precharge circuit for precharging said bitlines, said bitline ~~recharge~~ precharge circuit responsive to said third delayed clock ; and

providing a column select circuit for selecting particular bitlines to connect to means for outputting data signals from said array, said column select circuit responsive to said second delayed clock signal and said means for outputting data signals responsive to said fourth delayed clock signal.

Claim 25. (ORIGINAL) The method of claim 24, wherein said means for generating said first, second, third and fourth delayed clock signals are multiple stage delay circuits, each stage of each multiple delay stage circuit connected in series and each stage individually responsive to said control signal.

Claim 26. (ORIGINAL) The method of claim 25, wherein each stage includes a inverter having an input and an output and a multiplicity of capacitors connectable between said output of said inverter and ground by pass gates, each pass gate responsive to a different bit of said control signal.

Claim 27. (ORIGINAL) The method of claim 24, wherein said fourth delayed clock signals is delayed more than said third delayed clock signal, said third delayed clock signals is delayed more than said second delayed clock signal and second delayed clock signals is delayed more than said first delayed clock signal.

Claim 28. (ORIGINAL) The method of claim 24, wherein said means for generating said first, second, third and fourth delayed clock signals comprises:

a first set of multiple stage delay circuits and first means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage circuit individually responsive to said control signal, said means for selecting responsive to a first fuse signal generated by a first fuse bank circuit based on a pattern of blown and un-blown fuses in a first fuse bank;

a second set of multiple stage delay circuits and second means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage circuit individually responsive to said control signal, said means for selecting responsive to a second fuse signal generated by a second fuse bank circuit based on a pattern of blown and un-blown fuses in a second fuse bank;

a third set of multiple stage delay circuits and third means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage circuit individually responsive to said control signal, said means for selecting responsive to a third fuse signal generated by a third fuse bank circuit based on a pattern of blown and un-blown fuses in a third fuse bank; and

a fourth set of multiple stage delay circuits and fourth means for selecting one of said multiple stage delay circuits, each multiple delay stage circuit having a different base delay, each stage of each multiple delay stage circuit connected in series and each stage of each multiple delay stage circuit individually responsive to said control signal, said means for selecting responsive to a fourth fuse signal generated by a fourth fuse bank circuit based on a pattern of blown and un-blown fuses in a fourth fuse bank.

Claim 29. (ORIGINAL) The method of claim 24, further including:

further delaying said first delayed clock signal in response to a first additional fuse signal generated by a first additional fuse bank circuit based on a pattern of blown and un-blown fuses in a first additional fuse bank;

further delaying said second delayed clock signal in response to a second additional fuse signal generated by a second additional fuse bank circuit based on a pattern of blown and un-blown fuses in a second additional fuse bank;

further delaying said third delayed clock signal in response to a third additional fuse signal generated by a third additional fuse bank circuit based on a pattern of blown and un-blown fuses in a third additional fuse bank; and

further delaying said fourth delayed clock signal in response to a fourth additional fuse signal generated by a fourth additional fuse bank circuit based on a pattern of blown and un-blown fuses in a fourth additional fuse bank.

Claim 30. (ORIGINAL) The method of claim 29, wherein said first, second, third and fourth patterns of blown and un-blown fuses and said first, second, third and fourth additional patterns of blown and un-blown fuses are determined by scanning in test patterns into scan chains coupled to said first, second, third and fourth fuse banks and said first, second, third and fourth additional fuse bank and measuring the performance of said eDRAM.